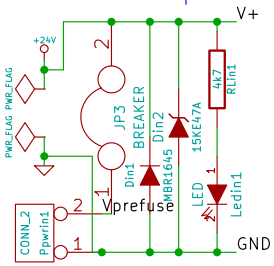
Reprap Development Board Interface: ww.reprap.org/wiki/RDB
Main interface board: RDB_STP_001_G_DIY_ADJ

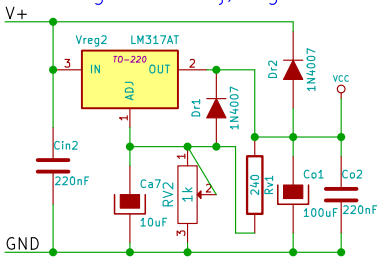
OSHW GLPv3

Power input



MBR or SPST diode current > fuse, Vbr min = Vin*1.3
15KEA transil unidirectional Vbr min extra rating approx *1.2
For 40-56V inputs use LM317HV, transil 15KE68A, SPST/MBR1660

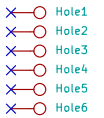
V.Regulator: adj, logic lvl

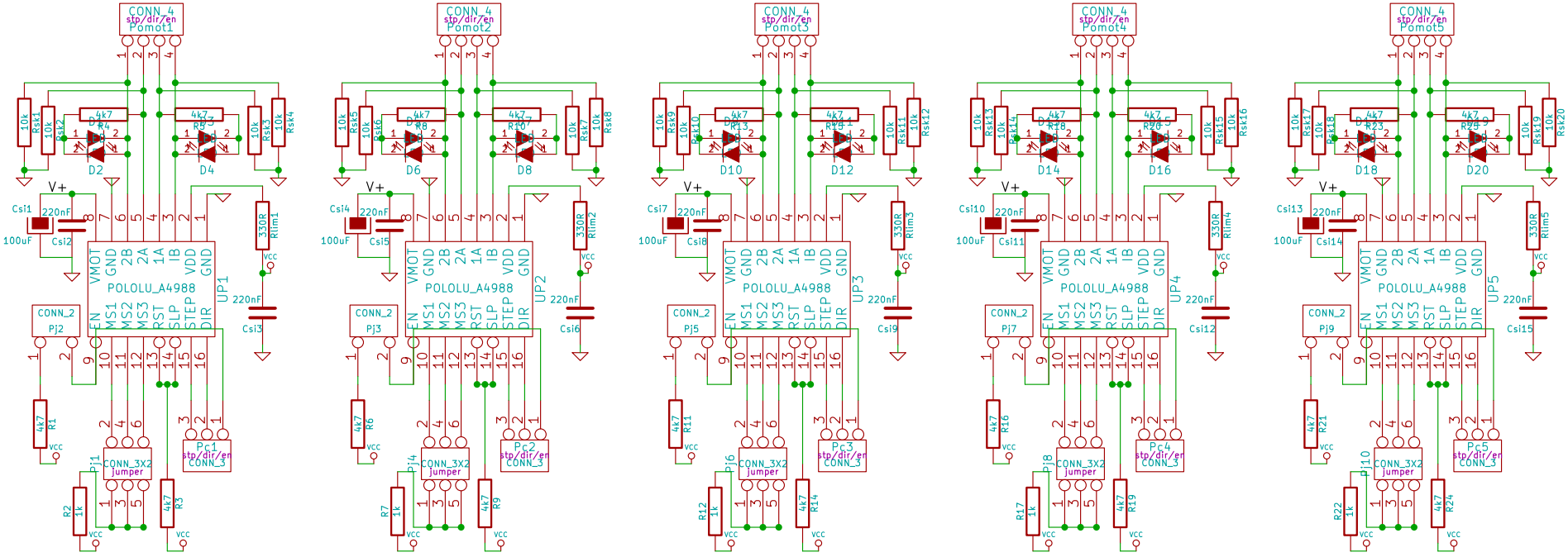


Set Voltage Regulator for logic level voltage.
If development board has its own onboard regulator then match it.
Most regulators 3pin, adj, TO220 are compatible (LM1086), but double check.

Power ends

Holes





ENABLE: to be low in normal operation, has 100k pulldown onboard (a4988), onchip 100k pulldown (drv8825)
SLEEP: to be high in normal operation & @startup, has 100k pullup onboard (a4988), onchip pulldown 1Mohm (drv8825)
RESET: to be high in normal operation, no default setting onboard (a4988), onchip pulldown 100k (drv8825)
MS: MS1, MS3 pins 100kΩ pulldown, MS2 50kΩ pulldown (a4988), all MS have 100k pulldown for drv8825
DRV8825: to keep faults from pulling sleep low, sleep pullup is 4k7 or less
External schottky diodes: SB540; SR540; 1N5822;

www.reprap.org/RDB		
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Sheet: /		
Title: RDB_STP_001_G_DIY_ADJ		
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